UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,644	05/19/2004	Mark D. Dupuis	BUR920040106US1	3643

30449 7590 12/01/2004

SCHMEISER, OLSEN + WATTS
SUITE 201
3 LEAR JET
LATHAM, NY 12033

EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,644	DUPUIS ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-14,21,28 and 29* is/are rejected.

7)☒ Claim(s) *2-7,15-20,22-27 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 8-11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Coolbaugh et al. (US 2002/0185708).

With reference to Figs. 2-4, the reference teaches the claimed invention in that it discloses a method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) forming a first region **16** of single crystal Si and a second region **12** of insulating material, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface (Fig.2) , and

(ii) depositing SiGe simultaneously on top of the first and second regions so as to grow third region **26** of single crystal SiGe and fourth region **24** of polycrystalline SiGe from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows from the first common interface surface, wherein the first and third regions comprise a same material and have single-crystal atoms arrangement, wherein the first region has a different atoms arrangement than the fourth region, and wherein the step of depositing the growth material is performed under a first deposition condition (Fig. 4 and related text).

Note that independent claims 1 and 14 recite an "if" condition, which include an option where the first yield of the first plurality of identical semiconductor structures is within a pre-specified range, leading to a second run to form a second plurality of identical semiconductor structures being not carried out. In this instant, the reference reads on every limitation of the claims.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Emons et al. (US 6,100,152).

With reference to Figs. 1-3, Emons teaches a method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) providing a silicon substrate (col. 3, lines 65-67);

(ii) forming a single-crystal silicon layer **3** on the substrate;

(iii) forming first and second shallow trench isolation regions **8** in the single-crystal silicon region **3**, the first and second shallow trench isolation regions defining a first single-crystal silicon region **3** sandwiched between the first and second shallow trench isolation regions;

(iv) growing a seed layer **4** of polysilicon on top of the first and second shallow trench isolation regions **8** (Fig. 1);

(v) depositing silicon and germanium simultaneously (A) on top of the first single-crystal silicon region **3** so as to grow a second single-crystal silicon region **1A** and (B) on top of the first and second shallow trench isolation regions **8** so as to grow first and second polysilicon regions **1B**, respectively, wherein the second single-crystal silicon region **1A** and the first polysilicon region **1B** are in direct physical contact with each other, wherein the second single-crystal silicon region **1A** and the second polysilicon region **1B** are in direct physical contact with each other (Fig.3 and related text); and

wherein the step of depositing silicon and germanium is performed under a first deposition condition (paragraph bridging col. 4 and col. 5).

Note that the claim recites an "if" condition, which includes an option where the first yield of the first plurality of identical semiconductor structures is within a pre-specified range, and a second run to form a second plurality of identical semiconductor structures is not carried out. In this instant, the reference reads on every limitation of the claims.

4. Claims 28, 29, 31, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Emons et al. cited above.

Emons teaches method for determining a fabrication condition for a semiconductor structure design, the method comprising the steps of:

(a) providing a relationship between a yield of the semiconductor structure design, a deposition temperature, and a precursor flow rate, wherein the semiconductor structure design comprises:

(i) a first region **3** of single crystal Si and a second region **8&9** of oxide, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface (Fig. 1); and

(ii) a third region **1A** and a fourth region **1B** being on top of the first region **3** and the second region **8**, respectively, wherein the third region **1A** and fourth region **1B** are grown by a step of depositing a SiGe simultaneously on top of the first region **3** and the second region **8&9** such that a second common interface surface between the third region **1A** and fourth region **1B** grows

from the first common interface surface, wherein the first and third regions comprise a same material and have single-crystal atoms arrangement, wherein the first region has a different atoms arrangement than the fourth region, and wherein the step of depositing the growth material is performed under the deposition temperature and the precursor flow rate (Fig.3 and related text);

(b) selecting a target yield for the semiconductor structure design; and

(c) determining a desired deposition temperature and a desired precursor flow rate under which the step of depositing the growth material would form a plurality of identical semiconductor structures according to the semiconductor structure design having the target yield, wherein the desired deposition temperature and the desired precursor flow rate are determined based on the relationship.

Note the following interpretation to explain as to how the reference meets the claimed limitation: the disclosure at the paragraph bridging column 4 and 5 provides a relationship between a yield of the semiconductor structure design, a deposition temperature, and a precursor flow rate. That is, the composition of the gas and the growth conditions (gas flow and temperature) are determined in such a way that the epitaxial growth results in the semiconductor layer 1 comprises, within the first 40nm, SiGe with a germanium content of 20%. The target yield of

the semiconductor structure design is a semiconductor device contains the semiconductor layer 1 having the characteristic set forth above.

As for claims 29, 31, and 32, since the epitaxial growth under selected temperature and composition of the gas (gas flow) produces the semiconductor layer 1 having the characteristic set forth above (target yield), the target yield is maximum because the result is obtained as designed.

5. Claims 1, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Khater et al. (US 2004/0188797).

With reference to Figs. 2E- 2H, Khater teaches a method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) forming a first region **AA** of single crystal Si and a second region **STI** of insulating material, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface;

(ii) forming a seed layer **UP1** on top of the first region **AA** and the second region **STI** (Fig. 2E);

(iii) removing a portion of the seed layer on top of the first region **AA** (Fig. 2G);

(iv) depositing SiGe simultaneously on top of the first and second regions so as to grow third region **IB** of single crystal SiGe and fourth region **DP1** of polycrystalline SiGe from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows from the first common interface surface, wherein the first and third regions comprise a same material and have single-crystal atoms arrangement, wherein the first region has a different atoms arrangement than the fourth region, and wherein the step of depositing the growth material is performed under a first deposition condition (Fig. 2H and related text).

Note that independent claim 1 recites an "if" condition, which include an option where the first yield of the first plurality of identical semiconductor structures is within a pre-specified range, and a second run to form a second plurality of identical semiconductor structures is not carried out. In this instant, the reference reads on every limitation of the claims.

Allowable Subject Matter

6. Claims 2-7, 15-20, 22-27, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Each of dependent claims 2, 15 and 22 set forth the condition in which a second yield of the second plurality of identical semiconductor structures is performed, and the result is not within the pre-specified range of the target yield thus forming a third plurality of identical semiconductor structures under a third deposition condition.

Each of dependent claims 5, 6, 18, 19, 25 and 26 set forth the condition in which a first yield of the first plurality of identical semiconductor structures is performed, and the result is not within the pre-specified range of the target yield thus forming a second plurality of identical semiconductor structures under a second temperature (or pressure) having a relationship with the first temperature (or pressure) as recited in the claims.

Claim 30 is allowable because prior art does not teach or suggest the limitation regarding the step of providing the relationship between the yield of the semiconductor structure design, the deposition temperature, and the precursor flow rate as recited in the claim.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

11/25/04